

WHAT IS CLAIMED IS:

1. An emulation device comprising:
a serial scan testability interface having at least first and second scan paths; and
state machine circuitry connected and responsive to said second scan path generally operable for emulation control.
2. The emulation device of claim 1 wherein said serial scan testability interface includes an instruction register, and scan path selection circuitry responsive to said instruction register.
3. The emulation device of claim 2 wherein said serial scan testability interface includes a separate state machine connected to control said instruction register and having a sequence of states responsive to an externally supplied digital signal.
4. The emulation device of claim 1 wherein said serial scan testability interface comprises a JTAG interface.
5. The emulation device of claim 1 wherein said second scan path includes scan registers for holding respective emulation command codes.
6. The emulation device of claim 1 wherein said second scan path includes a scan register for holding domain locking signals.

7. The emulation device of claim 1 further comprising a processor and a logic circuit for connection to the processor, said logic circuit operable to produce a done signal representing that the processor is done executing an instruction, wherein said second scan path includes a scan register for holding a selection signal determining whether the state machine circuitry is to be responsive to the done signal.

8. The emulation device of claim 1 for use with a test clock and a functional clock for a processor circuit wherein said second scan path includes a scan register and said state machine circuitry includes a clock control circuitry coupling the test clock or the functional clock to the processor circuit depending on a signal in the scan register.

9. The emulation device of claim 1 for use with a test clock and a functional clock for circuitry having domains wherein said second scan path includes a scan register and said state machine circuitry includes clock control circuitry having respective outputs for the domains so that the clock control circuitry independently couples the test clock to one domain and the functional clock to another domain depending on the signal in the scan register.

10. The emulation device of claim 1 for use with circuitry having domains wherein said second scan path includes scan registers for holding command codes designating a selected domain and first and second command codes for the selected domain, wherein said state

machine includes emulation control code registers for each of the domains, selection circuitry coupling said scan registers to the emulation control code registers, and a state machine connected to operate the selection circuitry.

11. The emulation device of claim 1 for use with circuitry to be emulated producing a done signal indicative of a predetermined electrical condition of the circuitry, wherein said state machine circuitry has respective inputs for a start signal from the testability circuitry and for the done signal.

12. The emulation device of claim 1 wherein said testability circuitry includes a decoding circuit having an output signaling to said state machine circuitry when a particular scan path is selected.

13. The emulation device of claim 1 for use with a test clock connected to said testability circuitry and a functional clock connected to said state machine circuitry and further comprising a handshake synchronizer connected between said testability circuitry and said state machine circuitry to produce a start signal for said state machine circuitry in response to said testability circuitry.

14. The emulation device of claim 1 wherein said first scan path includes a boundary scan path.

15. The emulation device of claim 1 for use with circuitry including shift register latches wherein said

testability circuitry includes a third scan path interconnecting said serial register latches.

16. The emulation device of claim 1 for use with circuitry having domains, wherein said testability circuitry includes additional scan paths for each of the domains and said second scan path includes a serial register for lock signals, the emulation device further comprising switching circuits connecting the additional scan paths in response to the lock signals.

17. An electronic device comprising:

a semiconductor chip and an integrated circuit fabricated thereon;

a serial scan testability interface on-chip having at least first and second scan paths; and

state machine circuitry on-chip connected and responsive to said second scan path generally operable for emulation control of said integrated circuit.

18. The electronic device of claim 17 wherein said testability circuitry includes additional scan paths defining domains in the integrated circuit, and said second scan path includes a serial shift register for lock signals, the device further comprising switching circuits connecting the additional scan paths in response to the lock signals.

19. The electronic device of claim 17 wherein said second scan path includes scan registers for holding respective emulation command codes.

20. The electronic device of claim 17 wherein said integrated circuit includes a processor and a logic circuit connected to said processor, said logic circuit operable to produce a done signal for said state machine circuitry representing that the processor is done executing an instruction.

21. The electronic device of claim 17 further comprising a test clock and a functional clock wherein said second scan path includes a scan register and said state machine circuitry includes clock control circuitry coupling the test clock or the functional clock to the integrated circuit depending on a signal in the scan register.

22. The electronic device of claim 21 wherein said clock control circuitry has respective outputs for different domains in the integrated circuit so that the clock control circuitry independently couples the test clock to one domain and the functional clock to another domain depending on the signal in the scan register.

23. The electronic device of claim 17 wherein said testability circuitry has additional scan paths defining domains in the integrated circuit, said second scan path including scan registers holding command codes designating a selected domain and first and second command codes for controlling the selected domain, wherein said state machine circuitry includes emulation control code registers for each of the domains, selection circuitry coupling said scan registers to the emulation

control code registers, and a state machine connected to operate the selection circuitry.

24. The electronic device of claim 17 further comprising a circuit responsive to said integrated circuit to produce a done signal indicative of a predetermined electrical condition of the integrated circuit, wherein said state machine circuitry has respective inputs for a start signal from the testability circuitry and for the done signal.

25. The electronic device of claim 17 wherein said testability circuitry includes a decoding circuit having an output to signal to said state machine circuitry when a particular scan path is selected.

26. The electronic device of claim 17 including a test clock connected to said testability circuitry and a functional clock connected to said state machine circuitry and further comprising a handshake synchronizer connected between said testability circuitry and said state machine circuitry to produce a start signal for said state machine circuitry in response to said testability circuitry.

27. The electronic device of claim 17 wherein said first scan path includes a boundary scan path.

28. An electronic system comprising a printed wiring board and serial-scan interconnected electronic devices, each of the electronic devices including a semiconductor chip and an integrated circuit fabricated

thereon, a serial scan testability interface on-chip having at least first and second scan paths, and at least one of the electronic devices including state machine circuitry on-chip which is connected and responsive to said second scan path and generally operable for emulation control.

29. The electronic system of claim 28 wherein a said integrated circuit includes a processor and a logic circuit connected to said processor, said logic circuit operable to produce a done signal for said state machine circuitry representing that the processor is done executing an instruction.

30. The electronic system of claim 28 further comprising a test clock and a functional clock wherein said second scan path includes a scan register and said state machine circuitry includes clock control circuitry coupling the test clock or the functional clock to the integrated circuit depending on a signal in the scan register.

31. The electronic system of claim 30 wherein said clock control circuitry has respective outputs for different domains in the integrated circuit so that the clock control circuitry independently couples the test clock to one domain and the functional clock to another domain depending on the signal in the scan register.

32. The electronic device of claim 28 wherein said testability circuitry has additional scan paths defining domains in a said integrated circuit, said second scan

path including scan registers holding command codes designating a selected domain and first and second command codes for controlling the selected domain, wherein said state machine circuitry includes emulation control code registers for each of the domains, selection circuitry coupling said scan registers to the emulation control code registers, and a state machine connected to said selection circuitry.

33. An electronic system comprising a host computer, a serial scan interface associated with said host computer for downloading testability codes and emulation command codes, and an electronic system connected to said serial scan interface and including a printed wiring board and at least one electronic device that includes a semiconductor chip and an integrated circuit fabricated thereon, a serial scan testability interface on-chip having at least first and second scan paths for receiving said testability codes and emulation command codes respectively, and state machine circuitry on-chip which is connected and responsive to said second scan path and generally operable for emulation control.

34. The electronic system of claim 33 wherein said testability circuitry includes additional scan paths defining domains in the integrated circuit, and said second scan path includes a serial register for lock signals, the device further comprising switching circuits connecting the additional scan paths in response to the lock signals.

35. The electronic system of claim 34 wherein said domains include a domain including a processor core, a domain including peripheral circuitry, and a domain including analysis circuitry.

36. The electronic system of claim 33 wherein said second scan path includes scan registers for holding respective emulation command codes.

37. The electronic system of claim 33 wherein said integrated circuit includes a processor and a logic circuit connected to said processor, said logic circuit operable to produce a done signal for said state machine circuitry representing that the processor is done executing an instruction.

38. The electronic system of claim 33 further comprising a test clock and a functional clock wherein said second scan path includes a scan register and said state machine circuitry includes clock control circuitry coupling the test clock or the functional clock to the integrated circuit depending on a signal in the scan register.

39. The electronic system of claim 38 wherein said clock control circuitry has respective outputs for different domains in the processor circuit so that the clock control circuitry independently couples the test clock to one domain and the functional clock to another domain depending on the signal in the scan register.

40. The electronic device of claim 33 wherein said testability circuitry has additional scan paths defining domains in the integrated circuit, said second scan path including scan registers holding command codes designating a selected domain and first and second command codes for controlling the selected domain, wherein said state machine circuitry includes emulation control code registers for each of the domains, selection circuitry coupling said scan registers to the emulation control code registers, and a state machine connected to said selection circuitry.

41. A method of operating an emulation device comprising the steps of downloading testability codes and emulation command codes to respective scan paths of an integrated circuit, and sequentially executing the emulation command codes so that a first command code is executed and then a subsequent emulation command code is executed at a time depending upon completion of a predetermined electronic operation by the integrated circuit.

42. A method of operating an emulation device comprising the steps of downloading emulation command codes to a scan path of an integrated circuit, the emulation command codes identifying different ones of a plurality of domains of the integrated circuit and which of a test clock and a functional clock is to be applied to each domain, and executing the emulation command codes to couple the test clock or the functional clock to the domains of the integrated circuit in accordance with the emulation command codes.